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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/800,837	03/15/2004	David A. Klein	200309347-2	1528

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INTELLECTUAL PROPERTY ADMINISTRATION  
FORT COLLINS, CO 80527-2400

EXAMINER
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CERULLO, JEREMY S

ART UNIT	PAPER NUMBER
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2111

NOTIFICATION DATE	DELIVERY MODE
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09/16/2008

ELECTRONIC

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<b>Office Action Summary</b>	<b>Application No.</b> 10/800,837	<b>Applicant(s)</b> KLEIN ET AL.	
	<b>Examiner</b> Jeremy S. Cerullo	<b>Art Unit</b> 2111	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 June 2008.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-4,6-17,19-32,36-38,40-46 and 48-52 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4,6-17,19-32,36-38,40,45 and 46 is/are allowed.
- 6) ☒ Claim(s) 41-44,48 and 52 is/are rejected.
- 7) ☒ Claim(s) 49-51 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. Claims 1-4, 6-17, 19-32, 36-38, 40-46 and 48-52 are pending in the following action.

### ***Response to Arguments***

2. Applicant's arguments regarding Claims 41-44 and 48-52, filed 9 June 2008, have been fully considered but they are not persuasive.

3. While Claims 1-4, 6-17, 19-32, 36-38, 40, 45-46, and 49-51 are considered allowable in light of the Terminal Disclaimer and Amendments filed on 9 June 2008, Claims 41-44 have not been amended to include the allowable subject matter and the previous rejections are maintained. Also, newly presented Claims 48 and 52 do not include the allowable subject matter and have been rejected below.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 41-44, 48, and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,761,516 ("Rostoker" et al.), U.S. Patent No. 7,079,386 ("Jochym" et al.), and U.S. Patent Application Publication No. 2003/0088800 ("Cai") in view of what is old and well known in the art.

7. Rostoker teaches (Abstract; Figure 2; Column 3, Lines 9-58) an apparatus, a system comprising the apparatus, and a method for using the apparatus comprising a single-chip module (designed to replace a single processor module, having the same size and footprint), connected to a computer system as a single processor, comprising a plurality of processors processing data independently and simultaneously, cache control and bus bridge device (memory control / IO control) between the processors and the system bus (memory bus / IO bus) [as claimed in Claims 41, 44, 48, 52]. Rostoker does not teach the use of a fourth level shared cache in multiprocessor system [as claimed in Claim 43] or a method in a multiprocessor system for regulating the power consumption of a system by adjusting the operating frequencies of the processors. However,

Art Unit: 2111

Jochym teaches (Column 5, Lines 15-25) the use of a fourth level shared cache in a multiprocessor system [Claims 29 and 43] and Cai teaches (Paragraphs [0005]-[0007]) a multiprocessor system that comprises a method for regulating the power consumption of the system by adjusting the operating frequencies of the processors while maintaining an overall level of system performance. Also, Rostoker teaches (Column 3, Lines 9-16) that while the examples use Motorola and Intel X86 processors, invention is not limited to any particular combination of processors, but does not explicitly teach the use of Intel Itanium processors. The examiner takes OFFICIAL NOTICE that Intel Itanium processors are well known in the art, that it is well known in the art to include multiple processor modules in a computer system [Claim 52], and that it is well known to include power cabling in a computer system. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used the teachings of Rostoker, Jochym, and Cai using Itanium processors to create a power-efficient multiprocessor system on a single processor-style module.

8. Regarding Claim 41, the claimed elements are taught in the combination of references above as follows:

- a. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)
- b. Processors and cache control and bus bridge device in a module form such that the module is a drop-in replacement for a single processor module (Rostoker: Column 3, Lines 4-52)

Art Unit: 2111

- c. Processors process data independently (Rostoker: Column 3, Lines 42-52)
  - d. Module is a drop-in replacement (connects to a system board) for a single processor module (Rostoker: Column 3, Lines 4-52)
  - e. Use of a system bus (Rostoker: Figure 2, Item 72)
  - f. Processors process data independently (Rostoker: Column 3, Lines 42-52)
9. Regarding Claim 42, the claimed elements are taught in the combination of references above as follows:
- g. Power consumption equal to or less than that of a standard single processor module (Cai: Paragraphs [0002]-[0007])
10. Regarding Claim 43, the claimed elements are taught in the combination of references above as follows:
- h. Fourth-Level Cache (Jochym: Column 5, Lines 15-25)
11. Regarding Claim 44, the claimed elements are taught in the combination of references above as follows:
- i. Replacement for a single processor module (Rostoker: Column 3, Lines 4-52)
12. Regarding Claim 48, the claimed elements are taught in the combination of references above as follows:
- j. Plurality of logically independent processors (Rostoker: Figure 2, Items 54 and 56)

Art Unit: 2111

- k. Cache control and bus bridge device (Rostoker: Figure 2, Items 58 and 60)
- l. System bus (Rostoker: Figure 2, Item 72)
- m. Cache control and bus bridge device adapted to communicate with components such that the multiple processors are a single processor module (Rostoker: Column 3, Lines 4-52)

13. Regarding Claim 52, the claimed elements are taught in the combination of references above as follows:

- n. Plurality of similar apparatuses in computing device (Official Notice: it is well known in the art to include multiple processor modules in a computer system)

### ***Allowable Subject Matter***

14. Claims 1-4, 6-17, 19-32, 36-38, 40, and 45-46 allowed, in light of the Terminal Disclaimer and Amendments filed on 9 June 2008.

15. Claims 49-51 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Conclusion***

Art Unit: 2111

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy S. Cerullo whose telephone number is (571)272-3634. The examiner can normally be reached on Monday - Thursday, 8:00-4:00; Alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.



Art Unit: 2111

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. S. C./  
Examiner, Art Unit 2111

/MARK RINEHART/  
Supervisory Patent Examiner, Art Unit 2111